Docket No.: GR 98 P 8041

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German Priority Application No. 198 21 999.7, dated May 15, 1998.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

SOI semiconductor arrangement and method for fabricating the same

The invention relates to a semiconductor arrangement according to the preamble of claim 1 and, furthermore, to a method for fabricating such a semiconductor arrangement according to the preamble of claim 6.

It is already known to construct MOS field-effect transistors (MOSFETs) on silicon-on-insulator (SOI) substrates. A significant advantage of this technology is that, in comparison with conventional MOSFETs constructed on silicon substrates, it is possible to achieve complete electrical depletion of the channel during operation. The consequence of this is that very low operating voltages (below 1 V) can be achieved, which, in turn, makes it possible to realize "low-power" CMOS applications with a low power consumption. A further beneficial aspect of SOI technology is that very high packing densities can be realized on account of the both lateral and vertical insulation effect of the buried oxide layer. An up-to-date overview of SOI technology and its possible applications in the future is given in the article "Silicon-on-Insulator-Technologie: Neue "Low Power"-CMOS Anwendungen mit Betriebsspannungen kleiner 0.9 V", [Silicon-on-Insulator Technology: New "Low Power" CMOS Applications with operating voltages of less than 0.9 V], Pindl, S. and Risch, L., Phys. Bl. 54 (1998), No. 4.

In the case of conventional MOSFETs constructed on Si substrates, it is known that "hot charge carriers" can cause damage to the gate oxide. In this case, the "hot charge carriers" rupture Si-H bonds in the interface between the

channel silicon and the gate oxide and produce interface states (traps) which are undesirable because they lead to a change in various transistor parameters. The usual procedure for avoiding this so-called HC degradation (HC: hot carrier) is to provide a gentle transition in the drain doping. This measure, known as LDD doping (LDD: Lightly Doped Drain), reduces the production of hot charge carriers and hence damage to the gate oxide. What is disadvantageous, however, is that the transistor properties can be adversely influenced by the LDD doping.

The invention is based on the object of providing a semiconductor arrangement based on SOI technology which enables high-performance SOI transistors to be formed on it or which already comprises such high-performance SOI transistors. Furthermore, the aim of the invention is to specify a method for fabricating such a semiconductor arrangement.

The characterizing features of claim 1 are provided for achieving the first part of the formulation of the object.

The semiconductor arrangement according to the invention is thus comparable, in terms of its construction, with a conventional SOI substrate, but the passivating substance X is incorporated, with the formation of Si-X bonds, in the region of the interface between the insulation layer and the monocrystalline silicon layer arranged over the latter. Since the Si-X bonds have a greater bond energy than Si-H bonds, it is considerably more difficult for hot charge carriers to rupture them. Therefore, the Si-X bonds remain intact even in the event of comparatively high kinetic charge carrier energies, as a result of which the production of undesirable interface states in the transition region between the

insulation layer and the monocrystalline silicon layer is distinctly reduced.

If SOI transistors are formed in the semiconductor arrangement according to the invention by means of process steps that will subsequently be described in more detail, the consequence of the incorporation of passivating substance in accordance with the invention is that damage to the SOI insulation layer by hot charge carriers and associated impairment of transistor properties cannot occur, or can occur only to a very small extent.

The passivating substance X is preferably a halide and/or nitrogen. Both the halides, in particular fluorine and chlorine, and nitrogen form a bond with silicon whose bond energy is distinctly higher than the bond energy of the Si-H bond.

A particularly preferred embodiment of the invention is characterized in that laterally adjacent, differently doped regions are formed in the monocrystalline silicon layer, which regions form the source, channel and drain of a MOSFET, and in that a gate oxide layer is arranged above the channel region and an electrical connection structure forming the gate of the MOSFET is disposed over said gate oxide layer. In this case, the insulation layer creates insulation - which is resistant to HC degradation - of the source, channel and drain region of the SOI MOSFET with respect to the base layer and thus ensures a high transistor drain current.

In this case, an advantageous embodiment of the invention is characterized in that the passivating substance X is also incorporated in the region of an interface between the channel region of the monocrystalline silicon layer and the gate oxide

layer, with the formation of Si-X bonds. Not only the insulation layer but also the gate oxide layer is then passivated, i.e. protected from HC degradation. The concentration of the passivating substance X at the interfaces may be approximately 1018 cm-3 in this case.

The electrical insulation of adjacent MOSFETs can, in principle, be effected by one of the known technologies, for example LOCOS (Local Oxidation of Silicon) or STI (Shallow Trench Isolation). It is preferable, however, for adjacent MOSFETs to be electrically isolated from one another by Mesa insulation. In this technology, the silicon layer in the region between two SOI MOSFETs is removed down to the underlying insulation layer, in which case high packing densities can advantageously be obtained.

The second part of the formulation of the object according to the invention is achieved in accordance with the characterizing features of claim 6.

In the method according to the invention, the passivating substance X can be introduced into the insulation layer and/or the monocrystalline silicon layer either during or after the fabrication of the semiconductor structure. The subsequent heat treatment causes the introduced passivating substance X to diffuse into the region of the interface, where it replaces existing Si-H bonds by Si-X bonds.

The passivating substance X is preferably introduced by ion implantation into the corresponding layer(s). The ion implantation technique enables the passivating substance X to be deposited in a manner allowing a highly targeted dose and with positional accuracy. Furthermore, it is advantageous that the passivating substance X can be introduced into the

insulation layer through the upper monocrystalline silicon layer or else, if appropriate, further covering layers as well. Therefore, the introduction of the passivating substance X can chronologically succeed the fabrication of the SOI semiconductor structure, with the result that commercially available prefabricated SOI semiconductor structures can also be used as a basis for the method according to the invention.

The use of an implantation step for introducing the passivating substance X into an SOI semiconductor structure may be advantageous particularly when the SOI semiconductor structure is also fabricated by means of an ion implantation process. This is the case with the so-called SIMOX (Separation by Implementation of Oxygen) technology, in which the insulation layer is formed in the form of a buried SiO2 layer by implantation of a high oxygen dose into a monocrystalline silicon substrate. The implantation step for introducing the passivating substance X can then directly follow the oxygen implantation step for forming the SOI semiconductor structure, and, in a manner which is beneficial in terms of fabrication engineering, the two steps can be carried out in one and the same implantation installation. Furthermore, it is also possible to perform the passivating substance implantation step according to the invention prior to the oxygen implantation.

A further possibility is to introduce the passivating substance X into the SOI semiconductor structure by means of a diffusion step. A suitable fabrication method for this purpose, for SOI semiconductor structures, is known in the art as a BESOI (Bonded Etched-back Silicon on Insulator) method. In this method, two silicon semiconductor substrates are firstly provided in each case with a surface oxide layer. The two silicon semiconductor substrates are then joined by

contact-connection of their oxide layers and one of the silicon semiconductor substrates is removed, except for a thin residual layer, for the purpose of forming the upper monocrystalline silicon layer. In accordance with a design variant according to the invention, the BESOI method is now modified such that the passivating substance X is introduced into one or both oxide layers before the joining of the two silicon semiconductor substrates and/or into one of the silicon semiconductor substrates before or after the oxidation step. In this case, the introduction of the passivating substance X can be performed simply by thermal doping (diffusion of the passivating substance from a passivating substance gas into the corresponding layer), since the layers to be passivated are uncovered before the joining of the two silicon semiconductor substrates.

In order to obtain short diffusion paths in the heat-treatment step which is to be carried out after the introduction of the passivating substance X, it is expedient for the implantation maximum of the passivating substance X to be put in the vicinity of the interface with the monocrystalline silicon layer.

A covering oxide layer is preferably applied on the top monocrystalline silicon layer. This covering oxide layer may serve as a screen layer in subsequent implantation steps.

The introduction of the passivating substance X into the insulation layer and/or the monocrystalline silicon layer can be performed either before or after any patterning of the monocrystalline silicon layer that is to be carried out. One advantage of the last-mentioned possibility is that the passivating substance X, when being introduced into the insulation layer and/or the silicon layer, can simultaneously

be incorporated into so-called spacers which have been formed beforehand on steps of the patterned monocrystalline silicon layer. In this way, the spacers are passivated as well, as a result of which the formation of undesirable Mesa sidewall transistors can be effectively suppressed.

Further advantageous refinements of the invention are specified in the subclaims.

The invention is explained below, in an exemplary manner, using the description of four design variants of the method according to the invention with reference to the drawing: in the latter,

Figs. 1a to f show a first design variant, in which the passivating substance X is introduced prior to the patterning of the silicon layer by implantation into a buried oxide layer;

Figs. 2a to f show a second design variant, in which the passivating substance X is introduced prior to the patterning of the silicon layer by implantation into the silicon layer;

Figs. 3a to f show a third design variant of the invention, in which the passivating substance X is introduced after the patterning of the silicon layer by implantation into a buried oxide layer; and

Figs. 4a to f show a fourth design variant of the invention, in which the passivating substance X is introduced after the patterning of the silicon layer by implantation into the silicon layer.

According to Fig. 1a, an SOI semiconductor structure 5 comprises an Si base layer 1, which is formed by an Si substrate and is adjoined by a buried oxide layer 2, on which a monocrystalline silicon layer 3 is overlaid. By way of example, the SOI semiconductor structure 5 may be fabricated according to the SIMOX or BESOI technologies already mentioned and is commercially available as a finished product. Furthermore, the Si base layer 1 and the monocrystalline silicon layer 3 may already be p- or n-predoped by the manufacturer.

According to Fig. 1a, first of all a screen oxide layer 4 is formed on the SOI semiconductor structure 5. The screen oxide layer 4 may be formed for example by thermal oxidation of the monocrystalline silicon layer 3 or by deposition of a TEOS (tetraethyl orthosilicate) layer by means of a CVD method.

According to Fig. 1b, the passivating substance X is subsequently incorporated in a whole-area or large-area manner by implantation into the buried oxide layer 2. The implantation step is illustrated by arrows 6. By way of example, nitrogen, fluorine or chlorine is used as the passivating substance X. The incorporation process can be controlled in a highly targeted manner with regard to the incorporation depth, the incorporation dose and the incorporation profile. Since the passivating substance X is intended to be employed in the region of the interface 7 between monocrystalline silicon layer 3 and buried oxide layer 2, conditions which cause the implantation maximum 8 to lie a short way underneath the interface 7 are chosen in the implantation step.

A heat-treatment step is subsequently carried out. In the process, the passivating substance X implanted into the bur[redacted]

oxide layer 2 diffuses to the interface 7, the passivating substance distribution 8' also being shifted into the region of the interface 7. In the process, Si-H bonds present in the region of the interface 7 are replaced by the more energy-stable Si-X bonds. As a result, the damage resistance of the buried oxide layer 2 with respect to HC degradation is increased in the manner already described. Furthermore, the heat-treatment step effects annealing of damage or defects which have occurred during the implantation step in the upper layers 3 and 4. Fig. 1c illustrates the situation after the heat-treatment step has been carried out. The concentration of the passivating substance X may be approximately 1018 cm-3, for example.

Figs 1d to f show, in an exemplary manner, further process steps which are carried out for the patterning and insulation of the monocrystalline silicon layer 3 for the purpose of forming an SOI MOSFET. Such steps are also necessary to construct an integrated CMOS circuit on the SOI semiconductor structure 5. First of all, in accordance with Fig. 1d, the screen oxide layer 4 and the monocrystalline silicon layer 3 are removed, except for locally residual layer regions 3', 4', using customary photolithographic masking techniques and etching steps. As a result, the monocrystalline layer region 3' is electrically insulated from corresponding, adjacent layer regions (not illustrated in Fig. 1d). The method shown here is known as Mesa insulation in the art. Other insulation methods (for example LOCOS, STI) can also be employed instead of Mesa insulation.

According to Fig. 1e, the peripheral walls of the layer regions 3', 4' are covered with spacers 9. The spacers 9 serve to additionally insulate the peripheral walls of the free-standing layer regions 3', 4'.

Finally, according to Fig. 1f, the channel doping of the SOI MOSFET to be produced is brought about by a further implantation step. The channel implantation step is indicated by the arrows 10.

The implantation steps (Fig. 1b, Fig. 1f) can be carried out in a positionally selective manner by using implantation masks (not illustrated). In particular, the passivating substance X can be implanted in a targeted manner for example only into n-channel transistors.

The second method variant illustrated in Figs 2a to 2f differs from the first method variant shown in Figs 1a to f essentially merely in the fact that the implantation maximum 8 lies in the monocrystalline silicon layer 3 rather than in the buried oxide layer 2. In this case, the implanted dose of the passivating substance X should lie below the amorphizing dose in silicon. According to Fig. 2c, in this variant the implanted passivating substance X diffuses both to the interface 7 between buried oxide layer 2 and monocrystalline silicon layer 3 and to an interface 11 between monocrystalline silicon layer 3 and screen oxide layer 4. As a result, after removal of the screen oxide layer 4 and subsequent growth of a gate oxide layer on the monocrystalline silicon layer 3, the latter still contains sufficient passivating substance X in the region near the interface to increase the resistance of the gate oxide layer as well with respect to damage caused by hot charge carriers.

The steps of patterning/insulation, spacer formation and channel implantation as illustrated in Figs 2d to 2f are carried out analogously to the steps illustrated in Figs 1d to 1f.

The heat-treatment step shown in Fig. 2c may also be carried out after the Mesa insulation (Fig. 2d) and the provision of the spacers 9 (Fig. 2e). In that case, the passivating substance X is situated only in those portions of the interfaces 7, 11 which are covered by the layer regions 3', 4', i.e. in the active regions. When spacers 9 made of silicon oxide and a nitrogen passivating substance X are used, the spacer inner walls adjoining the peripheral walls of the layer regions 3', 4' are also nitrided in this case. During the subsequent channel doping (Fig. 2f) this inhibits the outdiffusion of channel dopant into the spacers and consequently suppresses the formation of Mesa sidewall transistors in a desired manner.

Halogens used as passivating substance X, on the other hand, accelerate the diffusion of channel dopant, in particular boron, into spacers 9 formed from silicon oxide. In order to avoid sidewall transistors, Mesa spacers 9 formed from silicon nitride are used in this case.

In the case of the third design variant of the method according to the invention as illustrated in Figs 3a to 3f, the passivating substance X is introduced into the buried oxide layer 2 as in the case of the first design variant (Figs 1a to f). The corresponding implantation step is illustrated in Fig. 3d. In contrast to the first design variant, however, the patterning/insulation and also the formation of the Mesa spacers 9 and subsequent thermal oxidation of the monocrystalline layer region 3' for the purpose of forming the screen layer region 4' (see Figs 3a to c) eventually take place prior to the passivating substance implantation step in this case.

If the spacers 9 are composed of silicon oxide, the consequence of this is that the passivating substance X is also implanted into the Mesa spacers 9, since the implantation depth is smaller in silicon oxide than in monocrystalline silicon. As a result, the suppressing - which was described in the case of the second design variant - of Mesa sidewall transistors in the event of using nitrogen as passivating substance X takes place in this case as well. Fig. 3e shows the nitrogen distribution 8' resulting after the heat-treatment step in the region of the interface 7 and at the peripheral walls of the monocrystalline layer region 3'. In the event of using halogens as passivating substance, spacers 9 composed of silicon nitride should be used - as already described in connection with the second design variant.

Fig. 3f again shows the channel implantation step.

If the heat-treatment step illustrated in Fig. 3e is not carried out until after the channel implantation (Fig. 3f), the well photomask (not illustrated) used for the channel implantation can be used to mask the implantation of the passivating substance X as well, with no additional outlay. In this procedure, too, the passivating substance X is implanted into the Mesa spacers 9, provided that the latter are composed of silicon oxide.

Figs 4a to 4f show a fourth design variant of the method according to the invention. In this case, as in the case of the third design variant, the patterning/insulation, the Mesa spacer formation and the thermal oxidation of the active silicon layer region 3' (Figs 4a to 4c) take place before the introduction of the passivating substance X by an implantation step (Fig. 4d). In contrast to the third design variant, a lower implantation energy is chosen in this case, with the

result that the implantation maximum 8 lies within the monocrystalline Si layer region 3'. Implantation into the spacers 9 takes place in this case as well. Fig. 4e shows the distribution 8' of the passivating substance X after the heat-treatment step. The advantage of this design variant resides in the additional passivation (halogenation or nitriding) of the gate oxide to be grown on later (cf. the second design variant as well) and - given the use of nitrogen implantation and oxide spacers 9 - in the nitriding of the Mesa spacer inner side for the purpose of suppressing Mesa sidewall transistors. Fig. 4e shows that the active monocrystalline silicon layer region 3' is completely passivated on all sides.

If halogens are used as the passivating substance X, spacers 9 made of silicon nitride should again be used. In addition, as in the case of the third design variant, it is possible, during the masking of the passivating substance implantation step (Fig. 4d), to use the same mask as for the channel implantation step (Fig. 4f).

The table below shows the bond energies of silicon with hydrogen and also the passivating substances nitrogen, fluorine and chlorine. It is evident that the Si-X bond has a distinctly higher bond energy when the abovementioned passivating substances X are used than when hydrogen is used as the bonding partner.

Table: Bond energies of silicon bonds

Bond	Bond Energy [eV]
Si-H	3.1
Si-N	4.6
Si-F	5.7
Si-Cl	4.7

Patent claims

1. A semiconductor arrangement having
- a base layer (1) made of semiconductor material, said base layer being formed, in particular, by a substrate,
- an insulation layer (2) arranged above the base layer (1), and
- a layer (3, 3') made of monocrystalline silicon, said layer being arranged above the insulation layer (2) and adjoining the latter,
characterized
in that a passivating substance X is present, with the formation of Si-X bonds, in the region of the interface (7) between the insulation layer (2) and the monocrystalline silicon layer (3, 3'), and
in that the bond energy of the Si-X bond is greater than the bond energy of an Si-H bond.

2. The semiconductor arrangement as claimed in claim 1, characterized in that the passivating substance X is a halogen and/or nitrogen.

3. The semiconductor arrangement as claimed in either of claims 1 and 2, characterized
- in that laterally adjacent, differently doped regions are formed in the monocrystalline silicon layer (3, 3'), which regions form the source, channel and drain of a MOSFET, and
- in that a gate oxide layer is arranged above the channel region and an electrical connection structure forming the gate of the MOSFET is disposed over said gate oxide layer.

4. The semiconductor arrangement as claimed in claim 3, characterized in that the passivating substance X is furthermore present in the region of an interface (11) between

the channel region of the monocrysalline silicon layer (3, 3') and the gate oxide layer, with the formation of Si-X bonds.

5. The semiconductor arrangement as claimed in either of claims 3 and 4, characterized
- in that the semiconductor arrangement comprises a plurality of MOSFETs, and
- in that two adjacent MOSFETs are isolated from one another by Mesa insulation.

6. A method for fabricating a semiconductor arrangement constructed in accordance with one of the preceding claims, characterized by the following steps:
- fabrication or provision of a semiconductor structure (5) constructed from the base layer (1), the insulation layer (2) and the monocrystalline silicon layer (3);
- introduction of the passivating substance X into the insulation layer (2) and/or into the monocrystalline silicon layer (3, 3') either during or after the fabrication of the semiconductor structure (5); and
- carrying out of a heat-treatment step.

7. The method as claimed in claim 6, characterized in that the passivating substance X is introduced by ion implantation into the insulation layer (2) and/or into the monocrystalline silicon layer (3, 3').

8. The method as claimed in claim 7, characterized in that in the case of passivating substance X which is introduced into the insulation layer (2) the implantation maximum (8) of the passivating substance X is put in the vicinity of the interface with the monocrystalline silicon layer (3, 3').

9. The method as claimed in claim 6, characterized in that the passivating substance X is introduced into the semiconductor structure (5) as early as during the fabrication thereof, by means of the following steps:
- provision of two silicon semiconductor substrates;
- formation of a respective oxide layer on the two silicon semiconductor substrates;
- introduction of the passivating substance X into one or both of the oxide layers and/or introduction of the passivating substance X before or after the oxidation step into one of the silicon semiconductor substrates;
- joining of the two silicon semiconductor substrates by contact-connection of their oxide layers, and
- partial removal of one of the silicon semiconductor substrates for the purpose of forming the monocrystalline silicon layer (3, 3').

10. The method as claimed in one of claims 6 to 9, characterized in that a covering oxide layer (4, 4') is applied to the monocrystalline silicon layer (3, 3').

11. The method as claimed in one of claims 6 to 10, characterized in that the monocrystalline silicon layer (3, 3') is patterned by being etched away in regions down to the insulation layer (2) situated underneath.

12. The method as claimed in claim 11, characterized in that the patterning step is performed before or after the introduction of the passivating substance X into the insulation layer (2) and/or the monocrystalline silicon layer (3, 3').

13. The method as claimed in one of claims 6 to 12, characterized

- in that the monocrystalline silicon layer (3, 3') is doped differently region by region by means of ion implantation, and
- in that this doping step is performed after the introduction of the passivating substance X into the insulation layer (2) and/or the monocrystalline silicon layer (3, 3') and the heat-treatment step.

Abstract

SOI semiconductor arrangement and method for fabricating the same

A semiconductor arrangement has a base layer (1) made of semiconductor material, said base layer being formed, in particular, by a substrate, an insulation layer (2) arranged above the base layer (1), and a layer (3') made of monocrystalline silicon, said layer adjoining said insulation layer. A passivating substance is present, with the formation of Si-X bonds, in the region of the interface (7) between the insulation layer (2) and the monocrystalline silicon layer (3'), the bond energy of the Si-X bond being greater than the bond energy of an Si-H bond.

Figure 1e